Comparison between ATLAS forward microstrip detectors made on 6" <100> and 4" <111> crystal oriented silicon wafers

G. Casse, P.P. Allport, P.S.L. Booth, A. Greenall, J.N. Jackson, T.J. Jones, N.A. Smith, P.R. Turner
University of Liverpool, Oxford St., Liverpool L69 7ZE, UK
PACS 2940, 6180

Abstract

The noise seen by the front-end readout electronics of silicon microstrip detectors depends on the capacitive load on each channel and the shot noise due to the reverse current in the detector. Because of the short integration time of the LHC electronics (25 ns), the shot noise contribution is negligible as long as the current is kept to an acceptable level. However, any inter-strip capacitance increase after irradiation will degrade the noise performances of the detectors. A dependence of the capacitance on the crystal orientation of the silicon crystal used as a substrate for silicon detectors has been recently reported [1]. We present here the results of irradiation of silicon microstrip detectors made on 6" <100> and 4" <111> crystal oriented silicon wafers in term of inter-strip capacitance and noise, measured using LHC speed binary electronics (LBIC [2]), as a function of bias. A strong dependence of the inter-strip capacitance on the bias applied to the detector has been found for the irradiated detectors made on <111> silicon, but this dependence decreases with the frequency of the measurement. At high frequencies, which are the only ones relevant for the noise behaviour of the detectors, we found no differences at high bias voltages between the values before and after irradiation for detectors made on silicon with different crystal orientations. The effect on the noise has been checked and at the nominal operation bias we found no measurable differences between detectors made on silicon with different crystal orientations.

1. Introduction

The silicon detectors for the ATLAS semiconductor tracker (SCT) are designed to efficiently operate after a fluence of $3 \cdot 10^{14}$ protons cm^{-2}. Adequate operation is insured by requiring a signal to noise ratio (S/N) sufficient to allow full hit efficiency and negligible noise occupancy with binary readout electronics. After irradiation, a high bias voltage (350V) will insure almost full charge collection, keeping the signal level close to the pre-irradiation value. Increased noise level is then responsible for reduction in the S/N ratio of irradiated detectors. The main source of noise due to the detector in the electronics is the capacitive load on each readout channel, which is determined by the capacitance of each read-out strip to the back-plane and to the other strips. The inter-strip capacitance is dominated by that to the first and second neighbours on each side. The capacitance to the back-plane for the various detector geometries used for the ATLAS SCT detectors is between 0.25 to 0.35 pF/cm. The inter-strip capacitance is about three times higher and therefore constitutes the main contribution to the capacitive load.

We present the evaluation of the detector parameters (reverse current, inter-strip capacitance and noise) before and after irradiation, studying the impact of the use of 6" <100> and 4" <111> crystal oriented silicon wafers. The different crystal orientation, together with the oxide quality, can influence the density of trapped charges at the interface $Si\text{-}SiO_2$ in the inter-strip region and therefore the behaviour of the inter-strip capacitance.

2. Pre-irradiation measurements

Wedge shaped microstrip silicon detectors made by Hamamatsu Photonics [3] on 4'' <111> crystal oriented and by Micron Semiconductor [4] on 6" <100> n-type silicon wafers were used for this study. They all have 768 strips with variable strip pitch due to the wedge shape. The average strip pitch was ~ 60 µm for the Hamamatsu detectors and ~ 75 µm for Micron ones. Both manufacturers used high grade and high resistivity FZ silicon, so the pre-irradiation full depletion voltage was between 50 and 65 volts for all devices. The detectors were able to sustain 1000 V bias, with a total reverse current of a few µA or less.
The detectors were glued to ceramics support frames and bonded to rebondable modules to be connected to 512 channels of binary readout electronics[5]. A pitch adaptor allowed the connection of the 768 strips to the 512 channels, pairing half of the strips together. The modules comprised a hybrid populated with four LBIC-CDP[6] chip sets. Figure 1 shows the schematic drawing of the binary electronics. The signal is amplified and shaped and the output level is compared with a reference threshold level (V_T) through a

discriminator, giving a binary 1 if the signal is above the threshold. The threshold can be varied from 0 up to a few volts. A threshold scan can be used to determine the performance of the system in terms of its response to a given input signal and its noise. Different charges can be injected at the input of the preamplifier via a calibration capacitor to determine the (signal dependent) gain.
The typical *'S curve'* obtained for each channel is shown in Fig. 2. A fit with the complementary error function to this provides the response of the amplifier at zero signal (threshold voltage corresponding to 0.5 efficiency) and the noise of the system (FWHM of the derivative of the efficiency curve). Figure 3 shows the technique used to extract the noise value at each detector bias voltage. A threshold scan is run for different values of the injected charge to obtain the response curve and hence the gain of the amplifier as a function of the input charge is determined. The amplifier is designed with a reduced gain for high-injected charge to save power consumption. The input noise is evaluated by the measured output noise divided by the gain.
The final noise figure for microstrip detectors coupled to the electronics is dominated by the total strip capacitance. The noise increases linearly with the capacitive load, as shown in Fig. 4 with the noise measured using LBIC electronics with various detectors for different strip length. The slope is about 65 enc/pF (the detector were biased above full depletion for this measurement).
The behaviours of the inter-strip capacitance of non-irradiated <111> and <100> substrate detectors as a function of the applied bias voltage are shown in Fig. 5. The inter-strip capacitance is roughly flat for the <100> substrate as a function of voltage, whilst it slightly decreases for the <111> substrate. In both cases the inter-strip capacitance is independent of the frequency of the measurement.

3. Results after irradiation

The detectors were irradiated with 24 GeV/c protons in dry atmosphere (N_2) under bias (100V) and at –9 ^{o}C in the CERN PS facility. The final dose was $3 \cdot 10^{14}$ cm^{-2}. After irradiation they were annealed for 7 days at 25 ^{o}C, to simulate the anticipated annealing of the detectors at the LHC. Figure 5 shows the reverse current measured at -17 ± 1 ^{o}C for the two families of detectors up to 500 V. The measured value of the reverse current insures that the contribution of the shot noise to the total noise of the detector is negligible and indicates that no excess noise due to microdischarge should be anticipated [7].
Figure 7 shows the intestrip capacitance measured for the two types of silicon with different crystal orientation. The inter-strip capacitance of the Micron <100> device remains flat as the applied bias increases. Slight frequency dependence is also observed. Both these features are much more pronounced for Hamamatsu <111> detectors. Nevertheless, the inter-strip capacitance at 350 volts and 300 MHz after irradiation coincides with the pre-irradiation value.
After irradiation the noise, measured with binary electronics, is found to increase, compared to the pre-irradiation value, as shown in Fig. 8. The noise does not, however, show any definite trend with increasing bias for Micron <111> or for Hamamatsu <100> detectors, as far as the precision of the measurement allows one to estimate.

4. Conclusion

After irradiation, Micron <100> 6" detectors have flat inter-strip capacitance versus bias behaviour. Hamamatsu <111> 4" detectors have inter-strip capacitance dropping with voltage but this effect is much less pronounced at higher (300 MHz) frequency, and the asymptotic post-irradiation inter-strip capacitance agrees with the pre-irradiation value. The noise seen with LHC speed binary electronics does not show any measurable trend in line with the behaviour of the inter-strip capacitance but instead looks independent of the voltage for both detector types.
For the post-irradiation high-voltage operation of silicon detectors, the noise performance shows no discernible correspondence with the different inter-strip capacitance behaviours of the <111> 4" Hamamatsu and <100> 6" Micron detectors.

References

[1] L. Feld et al., Radiation induced changes in the Interstrip Capacitance of Silicon Microstrip Detectors, 4th ROSE workshop on Radiation Hardening of Silicon Detectors, CERN 2-4 Dec. 1998, Publ. in CERN/LEB 98-11 (697).

[2] E. Spencer et al., IEEE Trans. Nucl. Sci. NS-42 (1995) 796.
[3] Hamamatsu Photonics, 1126-1 Ichino-cho, Hamamatsu 435, Japan
[4] MICRON Semiconductor, 1 Royal Buildings, Marlborough Road, Lancing, Sussex BN15 8UN (UK) .
[5] D. Robinson et al. Nucl Instr. and Meth. A 426 (1999) 28-33.
[6] J. De Witt, A pipeline and bus interface chip for silicon strip detector read-out, Proc. IEEE Nucl. Sci.Symp., San Francisco, CA., Nov. 1993.
[7] T. Oshugi et al., Nucl. Inst. and Meth. A 342 (1994) 22-26.

Figure caption

Fig. 1 Diagram of the LHC speed binary electronics.
Fig. 2 Example of an efficiency vs threshold S-curve for the LBIC binary read-out electronics.
Fig. 3 Response of the binary electronics to different input signals, evaluation of the gain and of the input noise.
Fig. 4 Noise measured with LBIC electronics versus capacitive load. The noise was measured with various detectors with different strip length. The slope is about 65 enc/pF.
Fig. 5 Inter-strip capacitance as a function of the bias applied to the detector for non-irradiated 4'' Hamamatsu <111> and 6'' Micron <100> crystal oriented silicon.
Fig. 6 Reverse currents after $3 \cdot 10^{14}$ p cm^{-2} for <111> and <100> crystal oriented silicon microstrip detectors.
Fig. 7 Inter-strip capacitance as a function of the bias applied to the detector for 4'' Hamamatsu <111> and 6'' Micron <100> crystal oriented silicon after $3 \cdot 10^{14}$ p cm^{-2}.
Fig. 8. Noise vs bias for Micron <100> and Hamamatsu <111> silicon microstrip detectors after $3 \cdot 10^{14}$ p cm^{-2}.

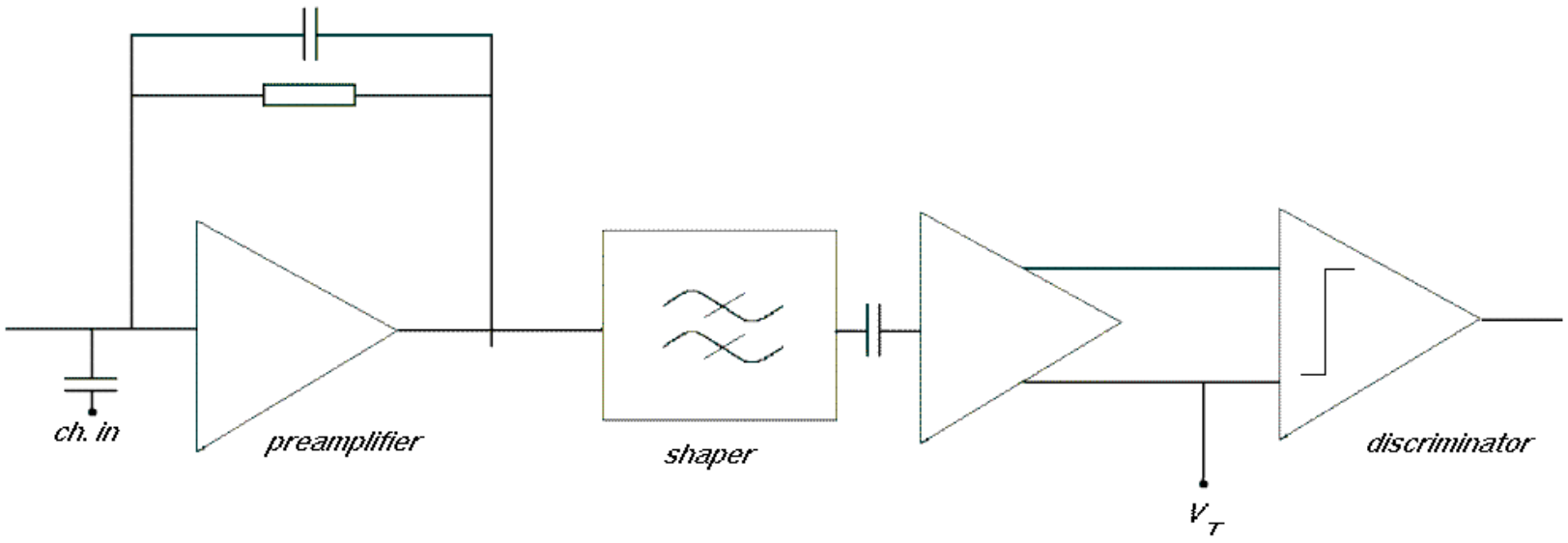


Fig. 1

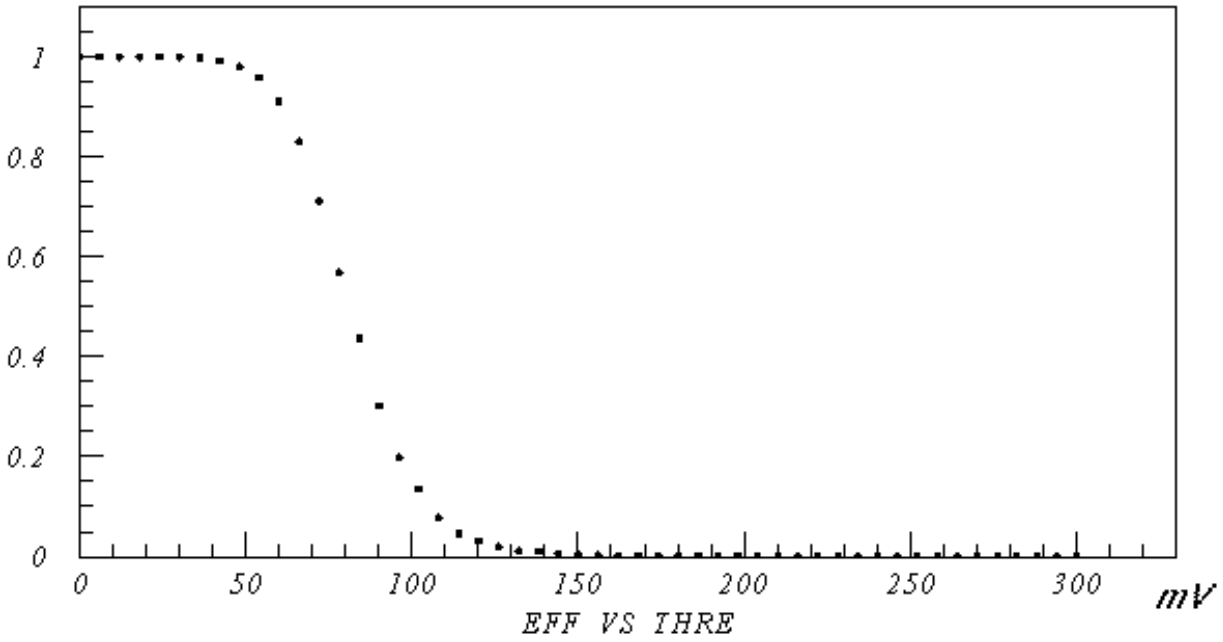


Fig. 2

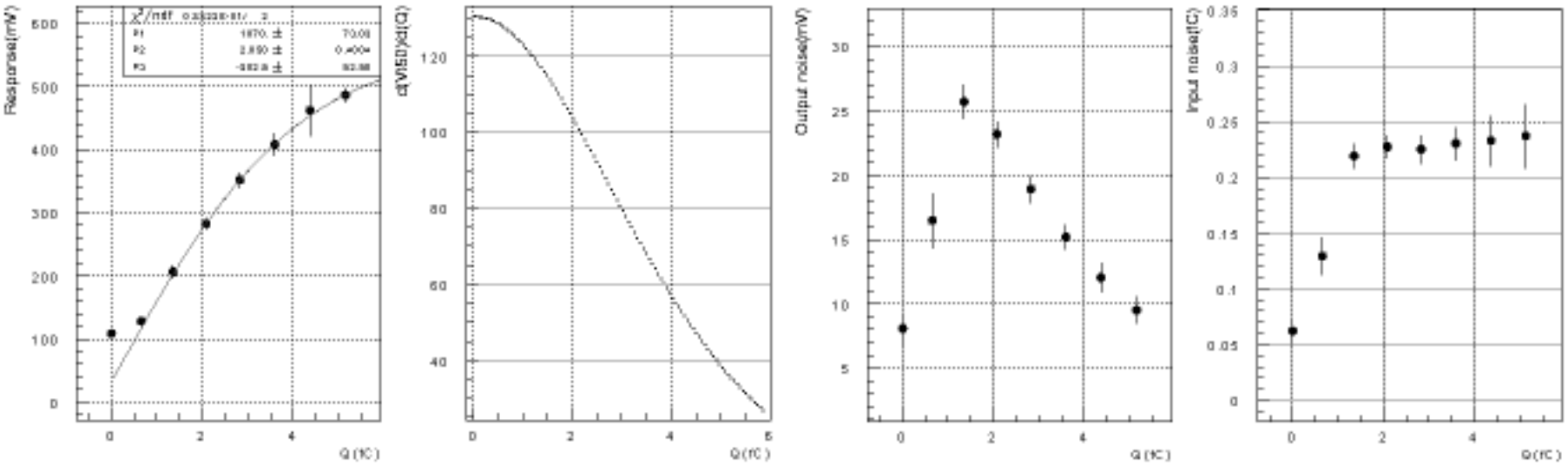

Response(mV)
Q (fC)
dV/dQ(mV/fC)
Q (fC)
Output noise(mV)
Q (fC)
Input noise(fC)
Q (fC)

Fig. 3

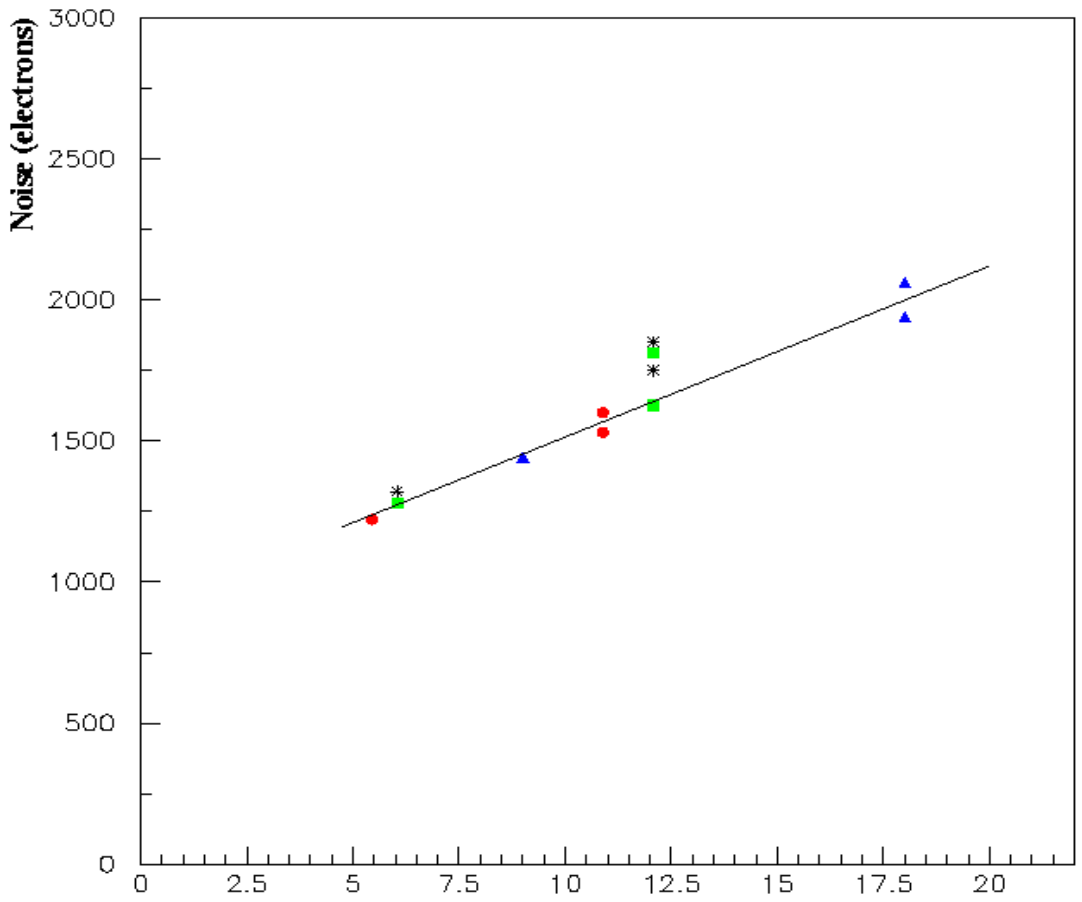
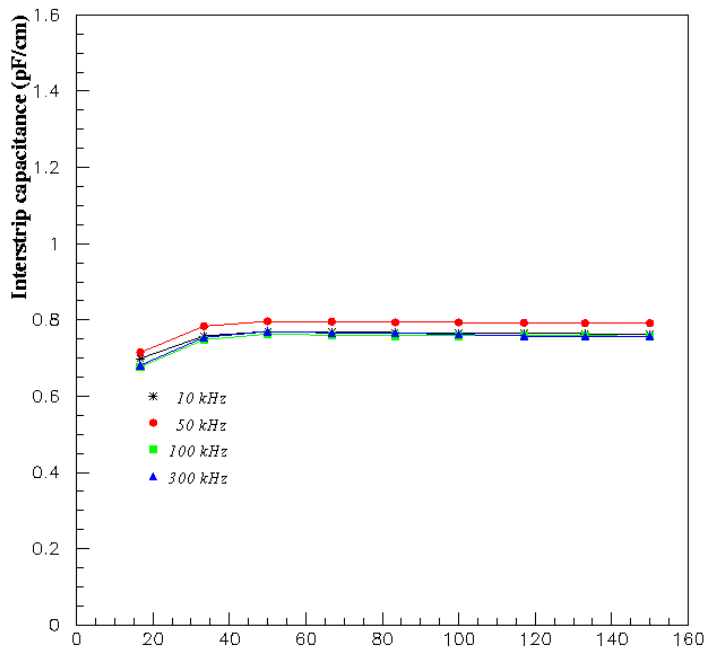

Noise (electrons)
3000
2500
2000
1500
1000
500
0
0
2.5
5
7.5
10
12.5
15
17.5
20

Fig. 4


Interstrip capacitance (pF/cm)
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
120
140
160
10 kHz
50 kHz
100 kHz
300 kHz

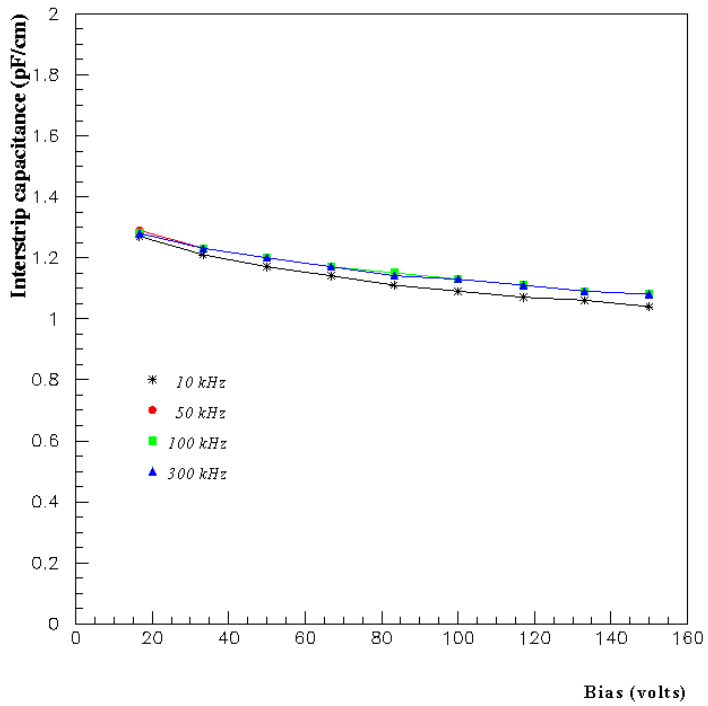
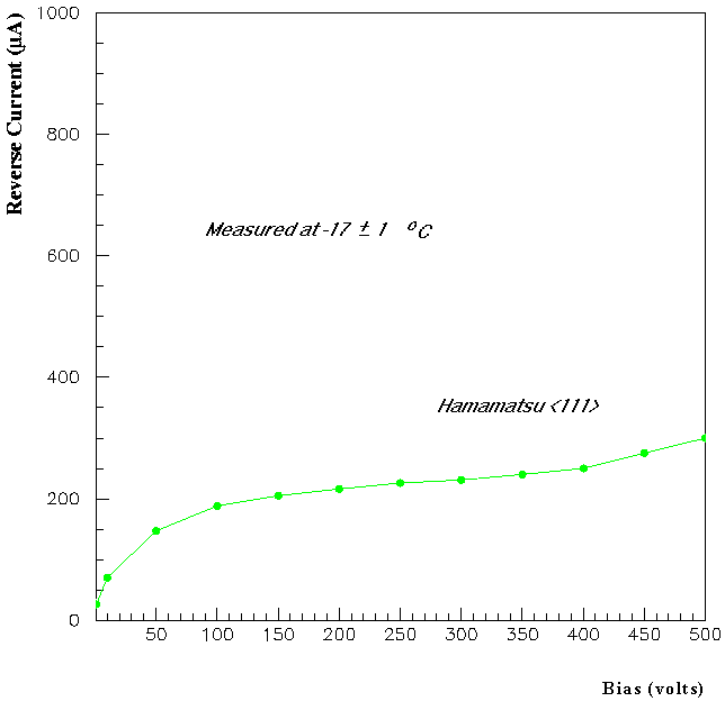

Interstrip capacitance (pF/cm)
2
1.8
1.6
1.4
1.2
1
0.8
0.6
0.4
0.2
0
0
20
40
60
80
100
120
140
160
10 kHz
50 kHz
100 kHz
300 kHz
Bias (volts)

Fig. 5


Reverse Current (µA)
1000
800
600
400
200
0
Measured at -17 ± 1 °C
Hamamatsu <111>
50
100
150
200
250
300
350
400
450
500
Bias (volts)

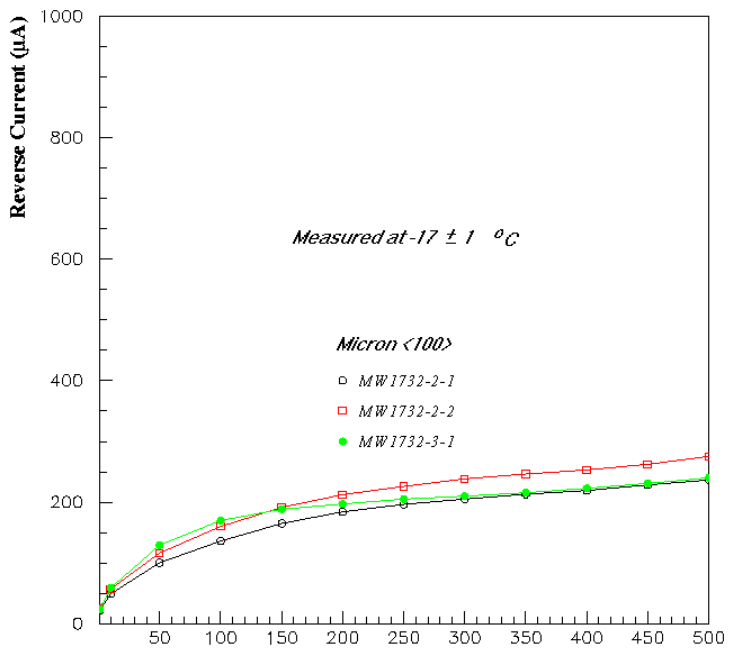
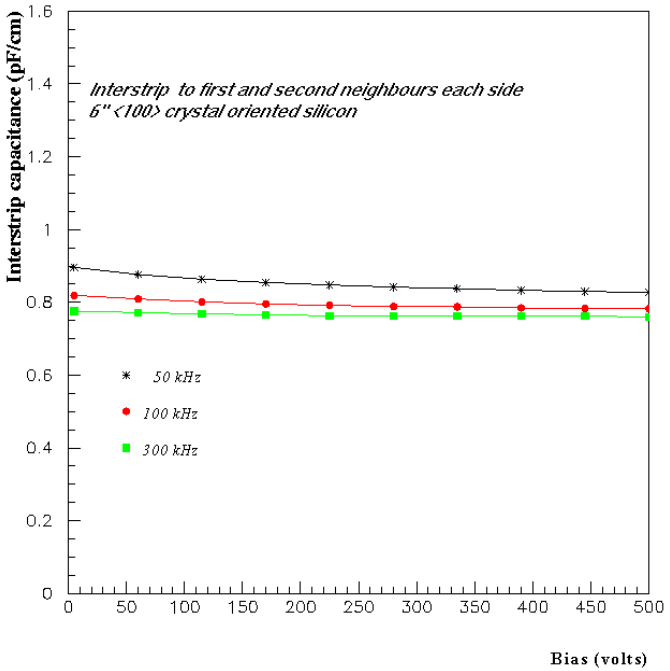

Reverse Current (µA)
1000
800
600
400
200
0
Measured at -17 ± 1 °C
Micron <100>
MW1732-2-1
MW1732-2-2
MW1732-3-1
50
100
150
200
250
300
350
400
450
500

Fig. 6


Interstrip capacitance (pF/cm)
Interstrip to first and second neighbours each side
6" <100> crystal oriented silicon
50 kHz
100 kHz
300 kHz
Bias (volts)

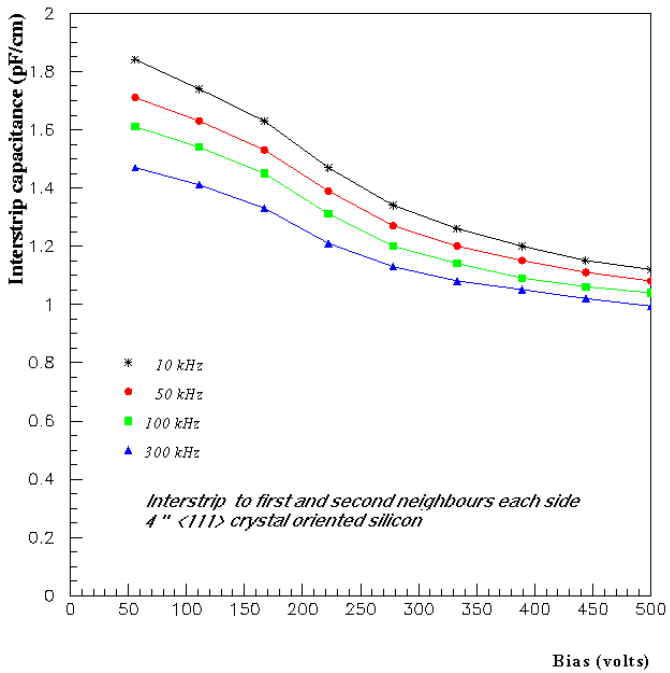

Interstrip capacitance (pF/cm)
10 kHz
50 kHz
100 kHz
300 kHz
Interstrip to first and second neighbours each side
4" <111> crystal oriented silicon
Bias (volts)

Fig. 7

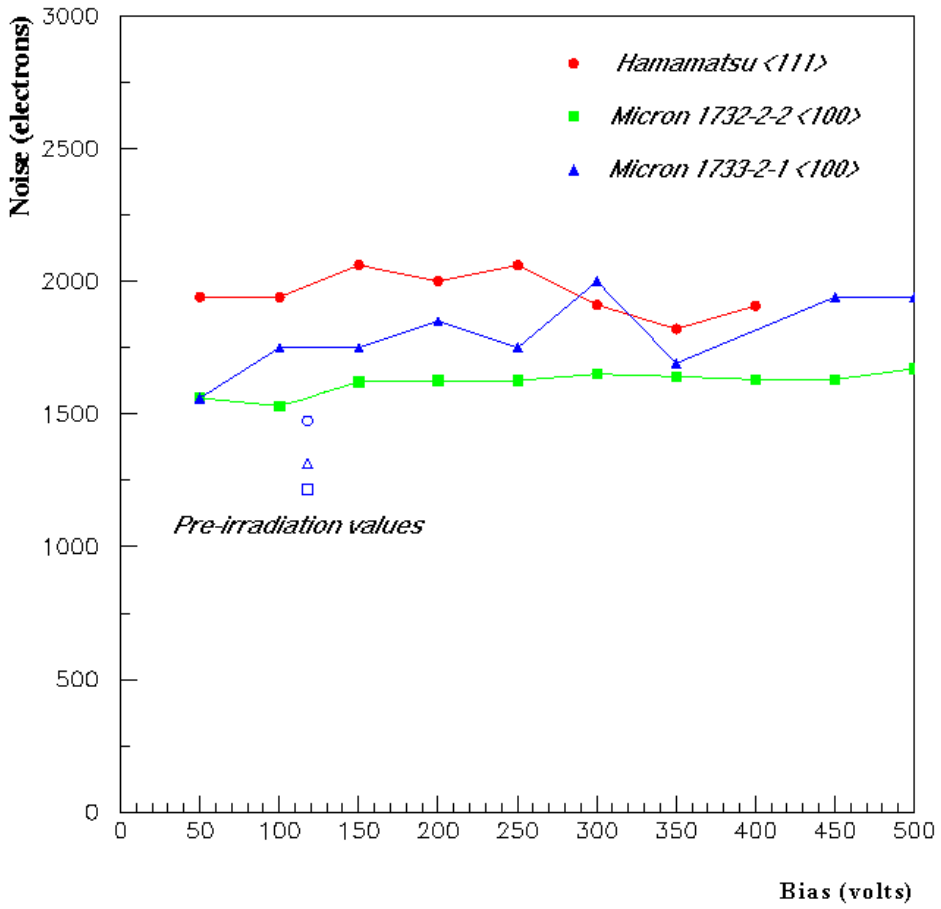

Noise (electrons)
3000
2500
2000
1500
1000
500
0
0
50
100
150
200
250
300
350
400
450
500
Bias (volts)
Hamamatsu <111>
Micron 1732-2-2 <100>
Micron 1733-2-1 <100>
Pre-irradiation values

Fig. 8